increasing an impurity concentration of the first conductive type in a thinned second side of the substrate so that a first conductive type layer is provided, wherein the impurity concentration of the first conductive type layer is higher than an impurity concentration of the first column, and

the first column provides a drift layer so that a vertical type first-conductive-type channel transistor is formed.

2. The method according to claim **1**, wherein

the first conductive type is a N conductive type, and the second conductive type is a P conductive type, and

the vertical type first-conductive-type channel transistor is a vertical type N channel transistor.

3. The method according to claim **1**, wherein

the forming the plurality of trenches includes:

measuring an impurity concentration of the substrate; and

measuring a width of each trench and a width between two adjacent trenches, and

in the forming the second conductive type semiconductor film, an impurity concentration of the second conductive type semiconductor film is controlled in such a manner that a product of the impurity concentration of the substrate and the width between two adjacent trenches is equalized to a product of the impurity concentration of the second conductive type semiconductor film and the width of the trench.

4. The method according to claim **1**, wherein

in the forming the second conductive type semiconductor film, a temperature of the substrate is maintained to be a predetermined temperature.

5. The method according to claim **2**, further comprising:

forming the vertical type N channel transistor in a surface portion of the first column after the forming the second conductive type semiconductor film.

6. The method according to claim **2**, further comprising:

forming a plurality of vertical type N channel transistors in a surface portion of the substrate before the forming the plurality of trenches, wherein

the surface portion is to be the first column, and

in the forming the plurality of trenches, each trench is disposed between two adjacent vertical type N channel transistors.

7. The method according to claim **1**, wherein

the substrate includes a dopant of phosphorous, arsenic or antimony.

8. The method according to claim **1**, wherein

the substrate has an impurity concentration in a range between $1\times10^{15}cm^{-3}$ and 1×10^{18} cm^{-3}.

9. A method for manufacturing a semiconductor device comprising:

forming a plurality of trenches on a first side of a semiconductor substrate, wherein the substrate has a first conductive type;

forming a second conductive type semiconductor film in each trench so that the substrate between two trenches provides a first column, and the second conductive type semiconductor film in each trench provides a second column, wherein the first and second columns are alternately repeated along with a predetermined direction in parallel to the first side of the substrate;

thinning a second side of the substrate, the second side being opposite to the first side;

increasing an impurity concentration of a first part of a thinned second side of the substrate so that the first part provides a first conductive type layer; and

reforming a second part of the thinned second side of the substrate so that the second part provides a second conductive type layer, wherein

the first part of the thinned second side is adjacent to the second part of the thinned second side,

the impurity concentration of the first conductive type layer is higher than an impurity concentration of the first column,

the impurity concentration of the second conductive type layer is higher than an impurity concentration of the second column,

the first column on the first part of the thinned second side provides a drift layer so that a vertical type first-conductive-type channel transistor is formed, and

the second column on the second part of the thinned second side provides a drift layer so that a vertical type second-conductive-type channel transistor is formed.

10. The method according to claim **9**, wherein

the first conductive type is a N conductive type, and the second conductive type is a P conductive type,

the vertical type first-conductive-type channel transistor is a vertical type N channel transistor, and

the vertical type second-conductive-type channel transistor is a vertical type P channel transistor.

11. The method according to claim **9**, wherein

the forming the plurality of trenches includes:

measuring an impurity concentration of the substrate; and

measuring a width of each trench and a width between two adjacent trenches, and

in the forming the second conductive type semiconductor film, an impurity concentration of the second conductive type semiconductor film is controlled in such a manner that a product of the impurity concentration of the substrate and the width between two adjacent trenches is equalized to a product of the impurity concentration of the second conductive type semiconductor film and the width of the trench.

12. The method according to claim **9**, wherein

in the forming the second conductive type semiconductor film, a temperature of the substrate is maintained to be a predetermined temperature.

13. The method according to claim **10**, further comprising:

forming the vertical type N channel transistor in a surface portion of the first column after the forming the second conductive type semiconductor film.

14. The method according to claim **10**, further comprising:

forming a plurality of vertical type N channel transistors in a surface portion of the substrate before the forming the plurality of trenches, wherein

the surface portion is to be the first column, and

in the forming the plurality of trenches, each trench is disposed between two adjacent vertical type N channel transistors.

15. The method according to claim **9**, wherein

the substrate includes a dopant of phosphorous, arsenic or antimony.